IN THE CLAIMS

1. (Currently Amended) A method for processing bundled instructions through execution units of a processor, comprising the steps of:

determining a throughput mode of operation, based upon a configuration bit;

fetching a first bundle of singly-threaded instructions from a singly- or multiply-threaded program;

distributing the first bundle to a first cluster of the execution units for execution therethrough;

fetching a second bundle of singly-threaded instructions from the program; and

distributing the second bundle to a second cluster of the execution units for execution therethrough.

2. (Original) A method of claim 1, further comprising processing the first bundle within the first cluster.

3. (Original) A method of claim 1, further comprising processing the second bundle within the second cluster.

4. (Original) A method of claim 1, further comprising the step of architecting data from the first cluster to a first register file.

5. (Original) A method of claim 4, further comprising the step of committing architected state from the second cluster to the first register file.

6. (Original) A method of claim 4, further comprising the step of architecting data from the second cluster to a second register file.

7. (Original) A method of claim 1, the step of fetching the first bundle comprising decoding instructions into the first bundle of the singly-threaded instructions.

8. (Original) A method of claim 1, the step of fetching the second bundle comprising decoding instructions into the second bundle of the singly-threaded instructions.

9. (Currently Amended) A method of claim 1, further comprising the steps of:

selecting the configuration bit to specify a wide mode of operation;

fetching a third bundle of singly-threaded instructions from the program;

distributing the third bundle to the first and second clusters of the execution units for execution therethrough; and

bypassing data between the clusters, as needed, to facilitate processing of the third bundle through the clusters.

10. (Original) A method of claim 9, the step of bypassing utilizing a latch to couple the data between the clusters.

11. (Cancelled)

12. (Currently Amended) A method for processing bundled instructions through execution units of a processor, comprising the steps of:

determining a wide mode of operation, based upon a configuration bit;

fetching a first bundle of singly-threaded instructions from a singly- or multiply-threaded program;

distributing the first bundle to two or more clusters of the execution units for execution therethrough; and

bypassing data between the clusters, as needed, to facilitate processing of the first bundle through the clusters.

13. (Currently Amended) A method of claim 12, further comprising the steps of[.]:

selecting the configuration bit to indicate a throughput mode of operation;

fetching a second bundle of singly-threaded instructions from the program;

distributing the second bundle to one of the clusters for execution therethrough;

fetching a third bundle of singly-threaded instructions from the program; and

distributing the third bundle to another one of the clusters units for execution therethrough.

14. (Cancelled)

15. (Currently Amended) In a processor architecture of the type having two or more clusters of execution units for processing instructions, the improvement comprising:

a configuration bit for specifying a wide mode or a throughput mode of operation;

a thread decoder for grouping instructions of a singly- or multiply-threaded program into singly-threaded bundles and for distributing the bundles to the clusters according to ~~either a wide mode or throughput mode of operation~~ the configuration bit;

wherein the singly-threaded bundles are distributed across a plurality of clusters in the wide mode and each singly-threaded bundle is distributed to one of the clusters in throughput mode.

16. (Original) In a processor architecture of claim 15, the further improvement wherein each cluster comprises a core and register file.

17. (Cancelled)

18. (New) A method for processing bundled instructions through execution units of a processor, comprising the steps of:

determining, based upon a configuration bit, a throughput mode or wide mode of operation;

fetching a first bundle of singly-threaded instructions from a singly- or multiply-threaded program;

if in throughput mode of operation, distributing the first bundle to a first cluster of the execution units for execution therethrough;

if in wide mode of operation, distributing the first bundle to multiple clusters of the execution units for execution therethrough;

fetching a second bundle of singly-threaded instructions from the program;

if in throughput mode of operation, distributing the second bundle to a second cluster of the execution units for execution therethrough; and

if in wide mode of operation, distributing the second bundle to multiple clusters of the execution units for execution therethrough.